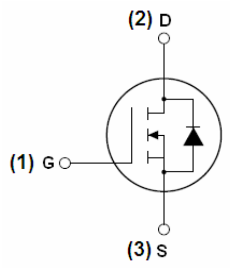
EFM4402

N-Channel Advanced MOSFET

• Product Summary

Part #	V_{DS}	$R_{DS(on).typ}$ (@V_{GS}=4.5V)	$R_{DS(on).typ}$ (@V_{GS}=2.5V)	I_D
EFM4402	20V	5.5mΩ	6.5mΩ	20A



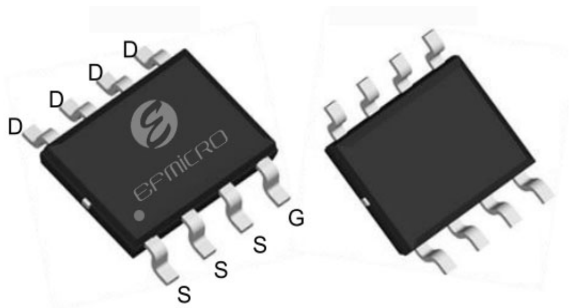
N-Channel MOSFET

• Description

- The EFM4402 is the high cell density trenched
- N-ch MOSFETs which provide excellent
- RDSON and gate cherge for most of the
- synchronous buck converter applications.
- The EFM4402 meet the RoHS and Green
- Prod uct requirement, 100 % EAS guaranteed
- with full function reliability approved.

•Application

- Super Low Gate Charge 100% EAS Guaranteed
- Green Device Available Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



SOP-8

•Ordering Information:

Part NO.	EFM4402
Marking	4402 ******
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

•Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	20	A
Drain Current-Pulsed (Note 1)	I_{DM}	140	A
Maximum Power Dissipation	P_D	3.1	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

•Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	75	℃/W

• Static Electrical Characteristics @ TJ = 25°C (unless otherwise stated)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250uA	20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V V_{GS}=0V	--	--	1	µA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V V_{DS}=0V	--	--	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} I_D=250uA	0.5	1.0	1.6	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V I_D=20A	--	5.5	6.5	mΩ
		V_{GS}=2.5V I_D=18A	--	6.5	8	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V I_D=20A	--	105	--	S
Gate Resistance	R_g	F=1.0MHz	--	1.4	--	Ω
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	V_{DS}=10V V_{GS}=0V F=1.0MHz	--	3860	--	PF
Output Capacitance	C_{oss}		--	740	--	PF
Reverse Transfer Capacitance	C_{rss}		--	580	--	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V I_D=20A V_{GS}=4.5V R_G=3Ω,	--	7	--	nS
Turn-on Rise Time	t_r		--	8	--	nS
Turn-Off Delay Time	$t_{d(off)}$		--	70	--	nS
Turn-Off Fall Time	t_f		--	18	--	nS
Total Gate Charge	Q_g	V_{DS}=10V I_D=12A V_{GS}=4.5V	--	36	--	nC
Gate-Source Charge	Q_{gs}		--	9	--	nC
Gate-Drain Charge	Q_{gd}		--	12	--	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V I_S=1A	--	0.75	1	V
Diode Forward Current (Note 2)	I_S		--	--	4	A

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

• Typical Characteristics

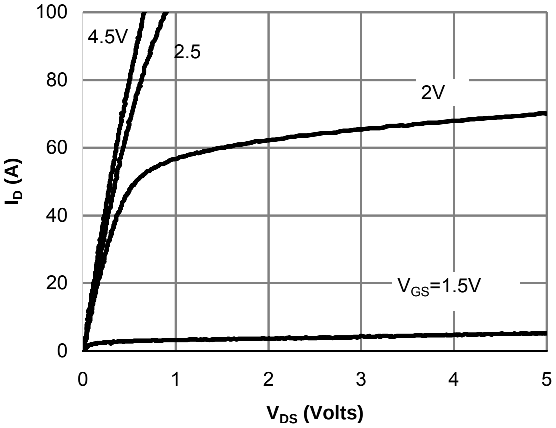


Fig 1: On-Region Characteristics (Note E)

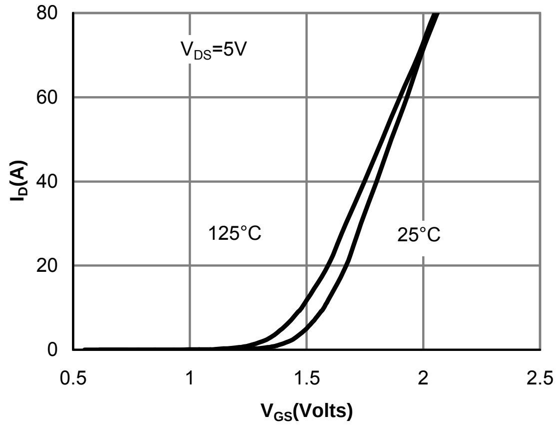


Figure 2: Transfer Characteristics (Note E)

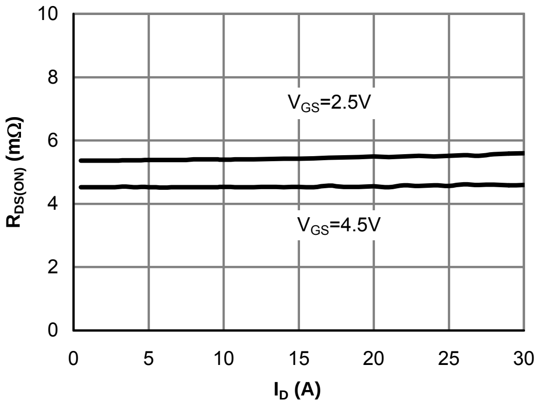


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

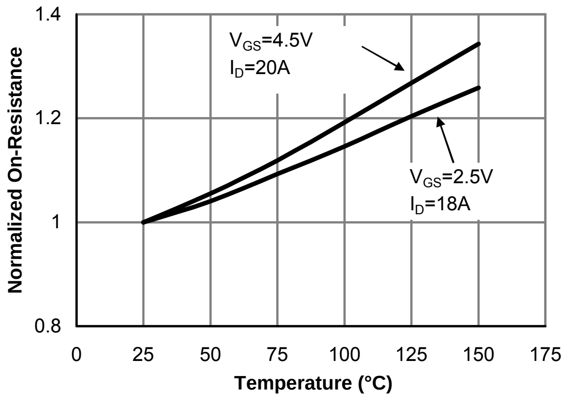


Figure 4: On-Resistance vs. Junction Temperature (Note E)

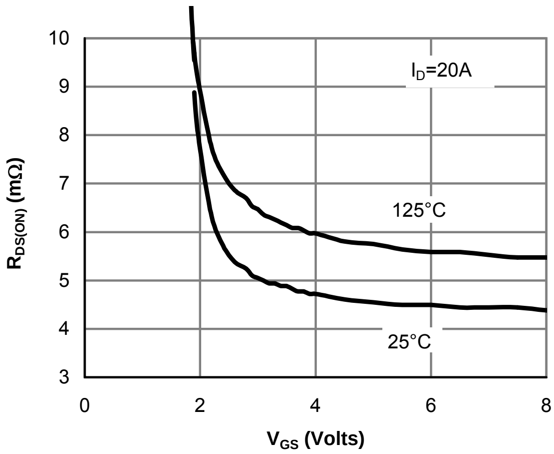


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

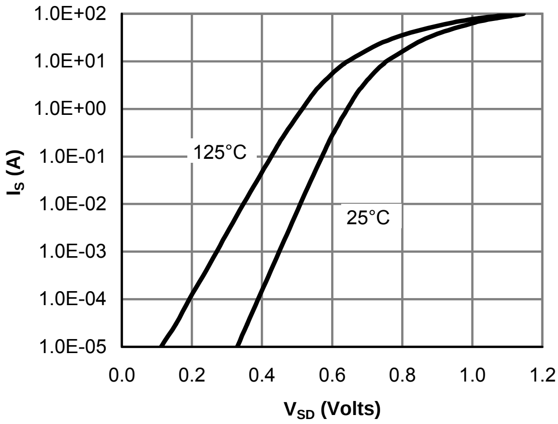


Figure 6: Body-Diode Characteristics (Note E)

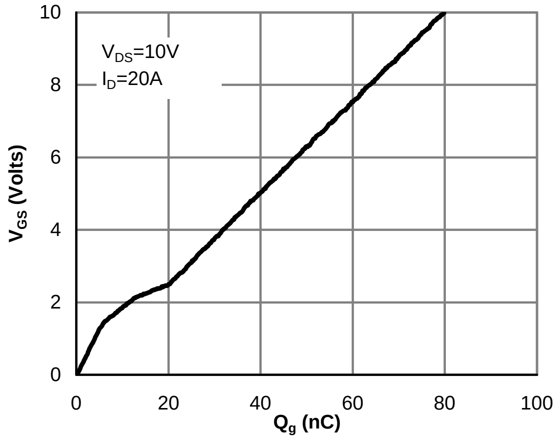


Figure 7: Gate-Charge Characteristics

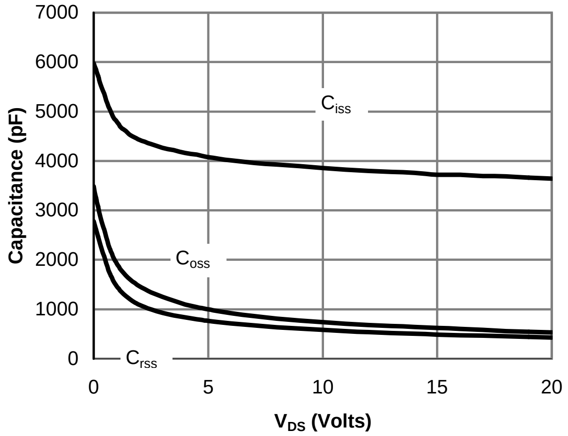


Figure 8: Capacitance Characteristics

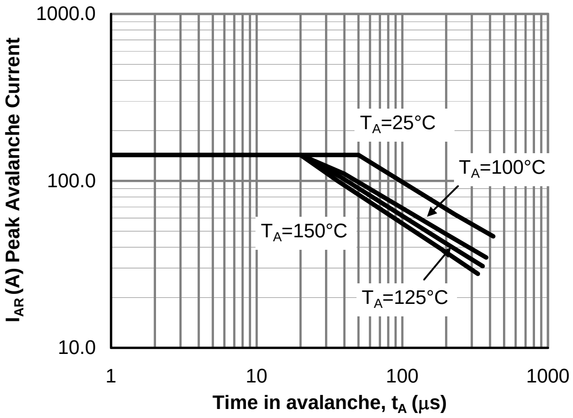


Figure 9: Single Pulse Avalanche capability (Note C)

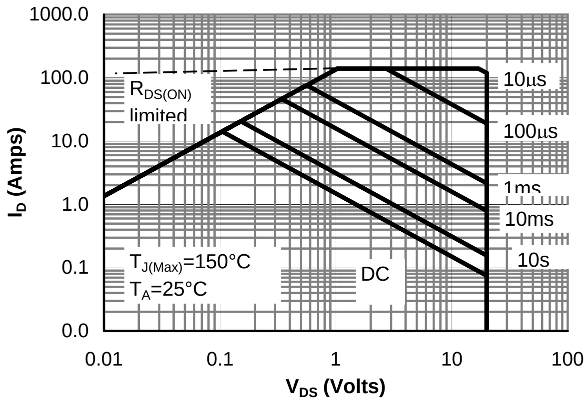


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

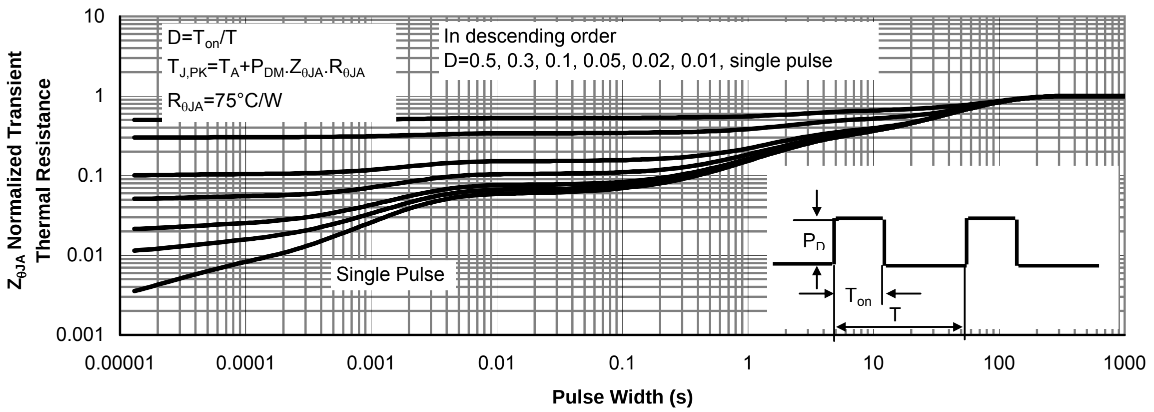
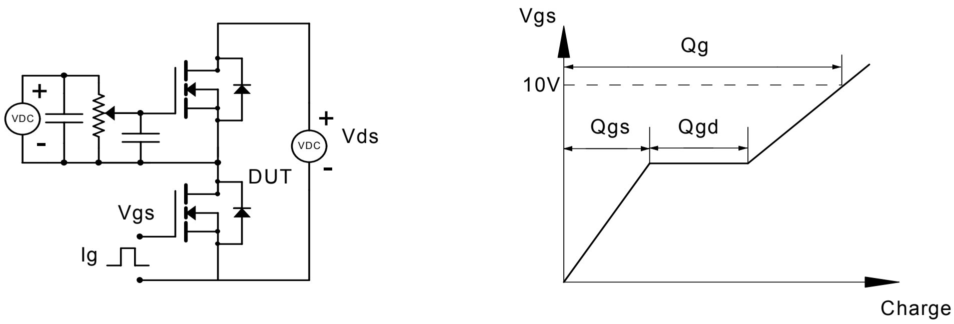


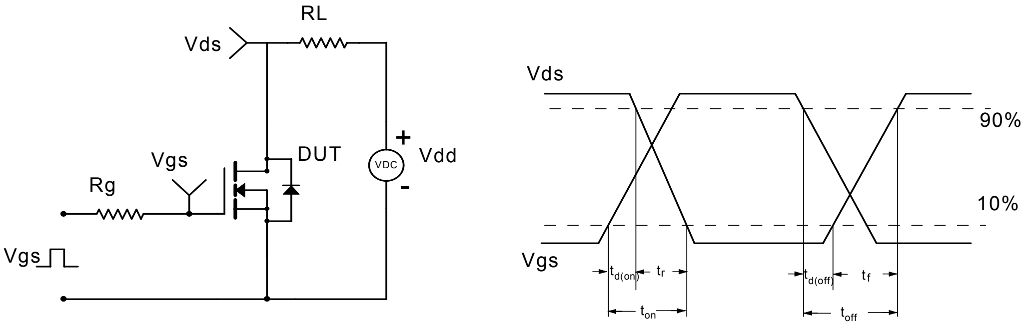
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

• Test circuit

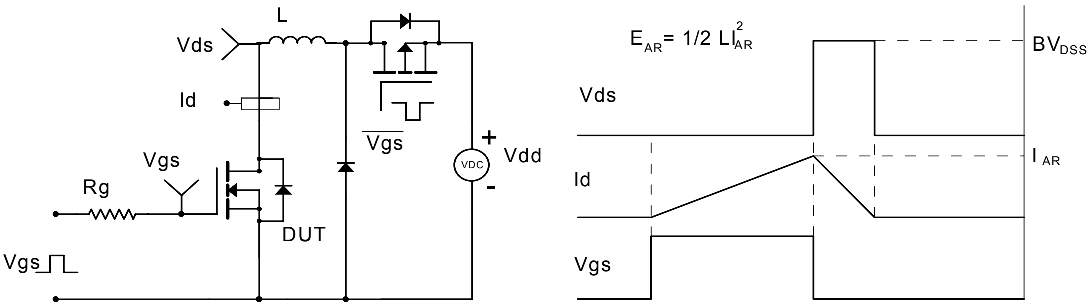
Gate Charge Test Circuit & Waveform



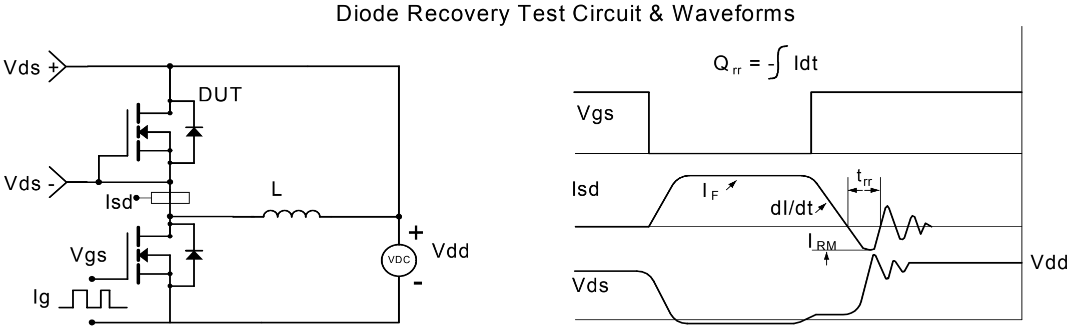
Resistive Switching Test Circuit & Waveforms



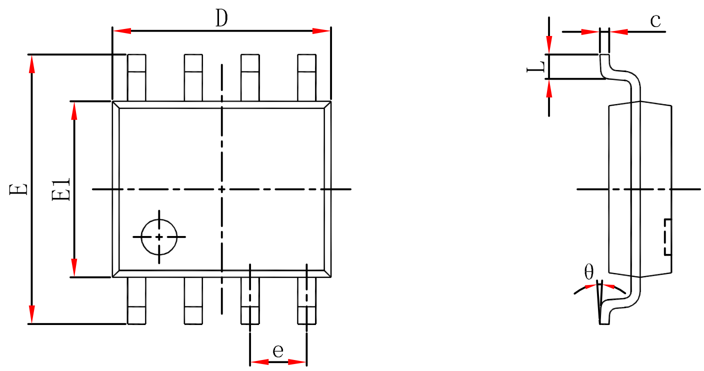
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

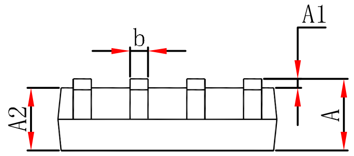


Diode Recovery Test Circuit & Waveforms

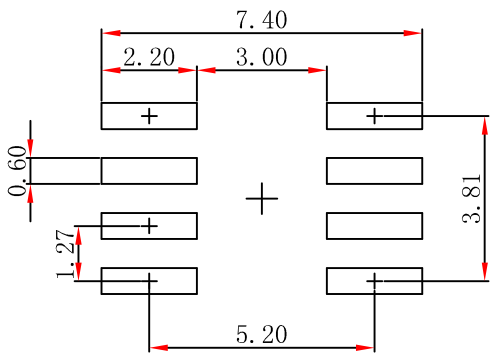


SOP8 Package Outline Dimensions





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
e	1.270（BSC）		0.050（BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.