

Product Summary

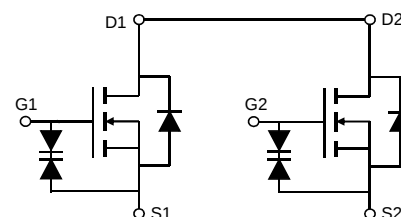
Part #	V_{DS}	$R_{DS(on).typ}$ (@ $V_{GS}=4.5V$)	$R_{DS(on).typ}$ (@ $V_{GS}=2.5V$)	I_D
EFM8820	20V	16m Ω	20m Ω	7A

Description

- The EFM8820 is the high cell density trenched
- N-ch MOSFETs which provide excellent
- RDSON and gate charge for most of the
- synchronous buck converter applications.
- The EFM8820 meet the RoHS and Green
- Product requirement, 100 % EAS guaranteed
- with full function reliability approved.

Application

- Super Low Gate Charge 100% EAS Guaranteed
- Green Device Available Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



N-Channel MOSFET



TSSOP-8

Ordering Information:

Part NO.	EFM8820
Marking	8820 *****
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	7	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	25	A
Maximum Power Dissipation	P_D	1.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	85	$^{\circ}C/W$
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• Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250uA	20	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V V _{GS} =0V	--	--	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V V _{DS} =0V	--	--	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =250uA	0.4	0.7	1.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V I _D =7A	--	16	20	mΩ
		V _{GS} =2.5V I _D =6.5A	--	20	24	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V I _D =7A	--	50	--	S

Dynamic Characteristics (Note4)						
Input Capacitance	C _{ISS}	V _{DS} =10V V _{GS} =0V F=1.0MHz	--	1295	--	PF
Output Capacitance	C _{OSS}		--	160	--	PF
Reverse Transfer Capacitance	C _{RSS}		--	87	--	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V I _D =7A V _{GS} =4.5V R _G =3Ω,	--	280	--	nS
Turn-on Rise Time	t _r		--	328	--	nS
Turn-Off Delay Time	t _{d(off)}		--	3.7	--	nS
Turn-Off Fall Time	t _f		--	2.3	--	nS
Total Gate Charge	Q _g	V _{DS} =10V I _D =7A V _{GS} =4.5V	--	10	--	nC
Gate-Source Charge	Q _{gs}		--	4.2	--	nC
Gate-Drain Charge	Q _{gd}		--	2.6	--	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V I _S =7A	--	0.75	1	V
Diode Forward Current (Note 2)	I _S		--	--	7	A

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

• Typical Characteristics

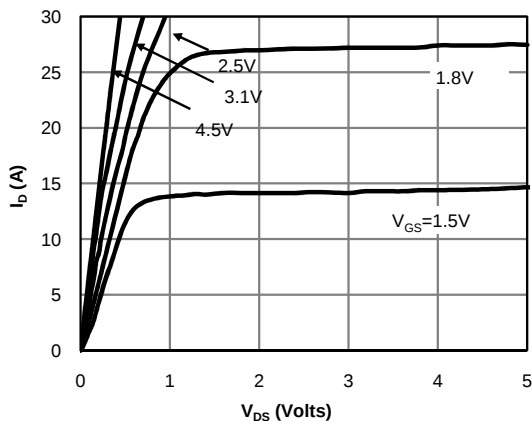


Figure 1: On-Region Characteristics (Note E)

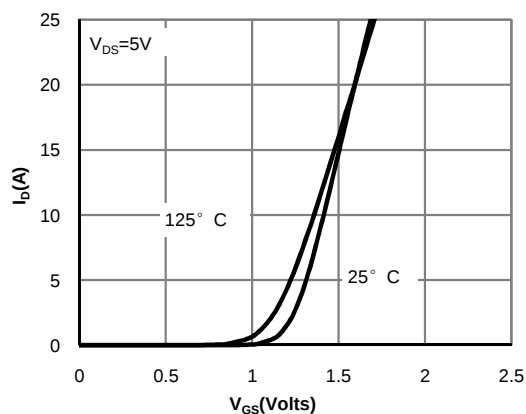


Figure 2: Transfer Characteristics (Note E)

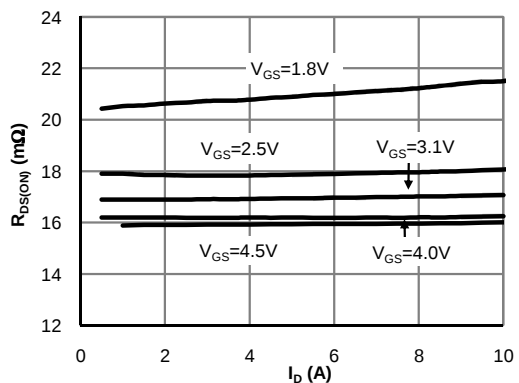


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

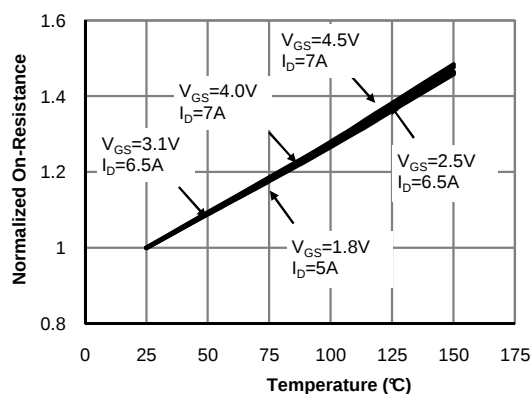


Figure 4: On-Resistance vs. Junction Temperature (Note E)

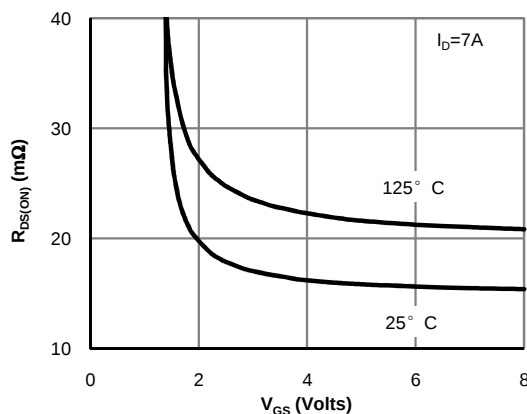


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

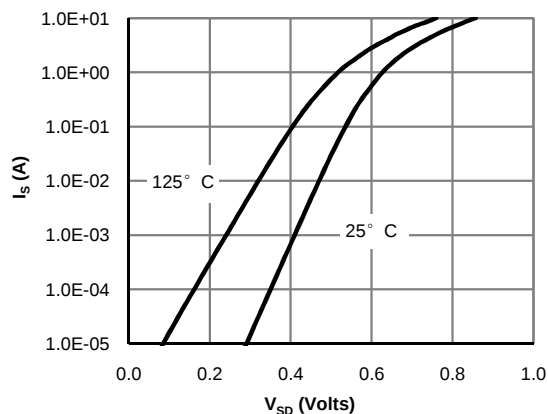


Figure 6: Body-Diode Characteristics (Note E)

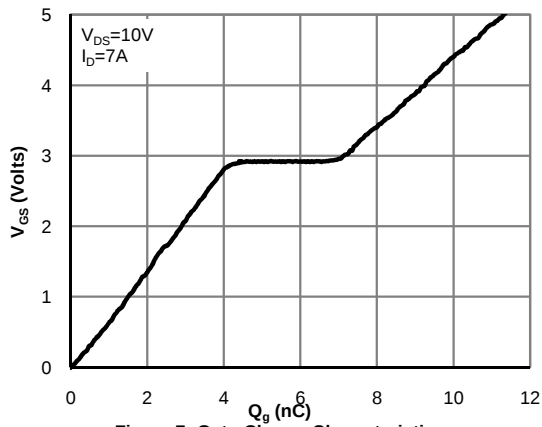


Figure 7: Gate-Charge Characteristics

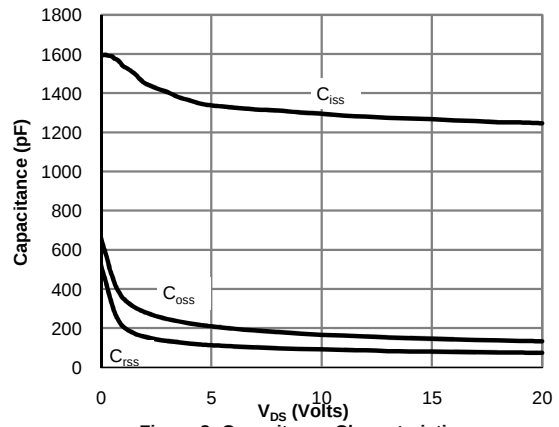


Figure 8: Capacitance Characteristics

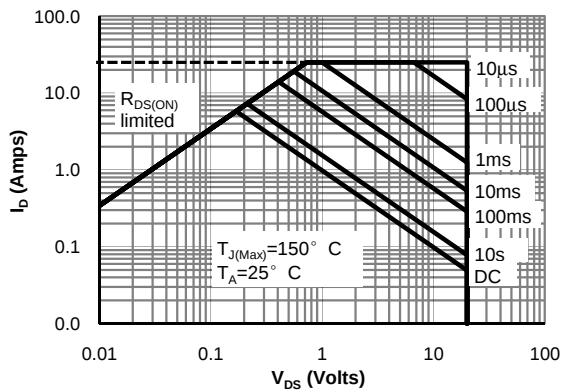


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

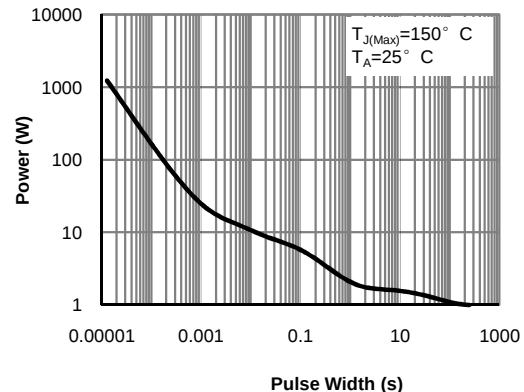


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

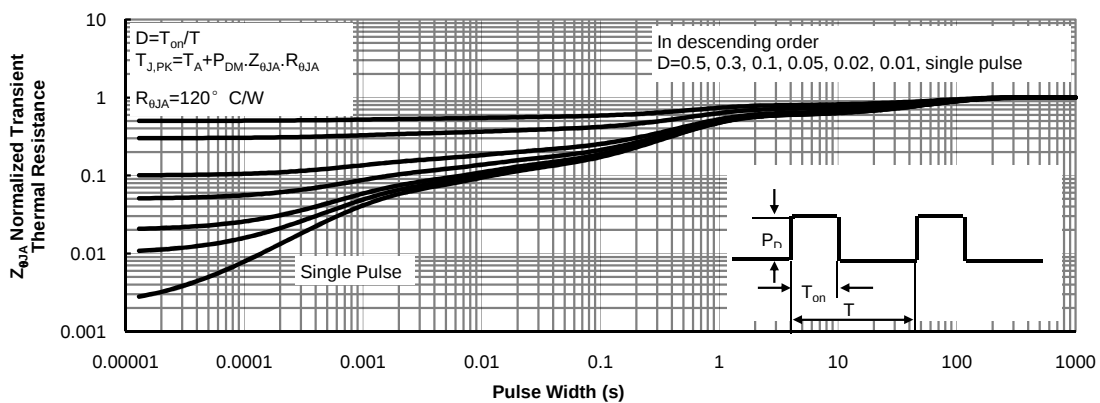
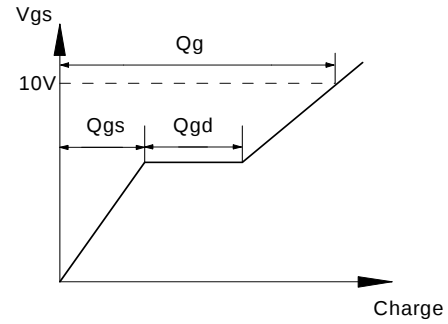
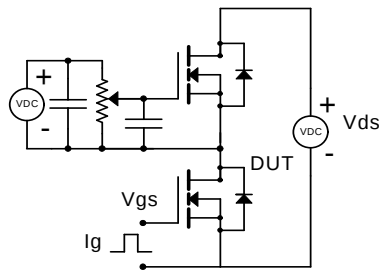


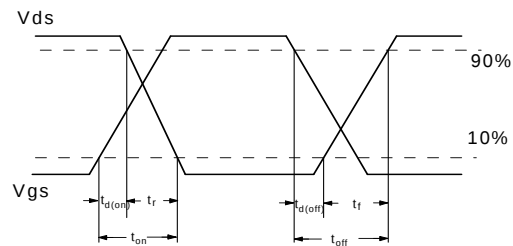
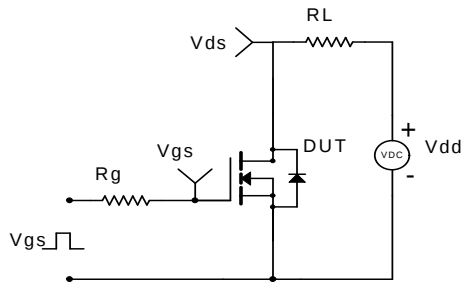
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

• Test circuit

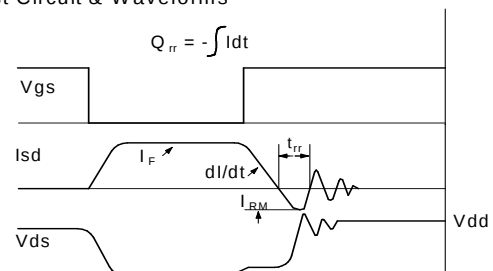
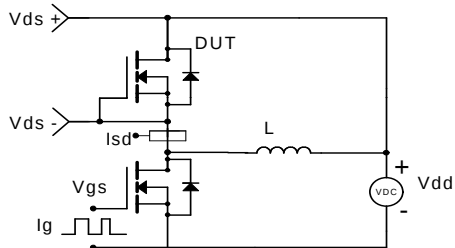
Gate Charge Test Circuit & Waveform



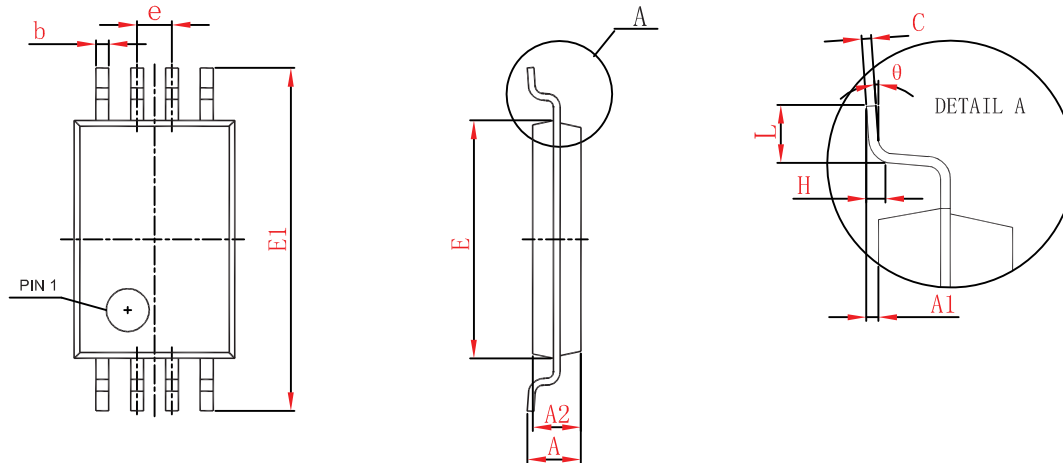
Resistive Switching Test Circuit & Waveforms



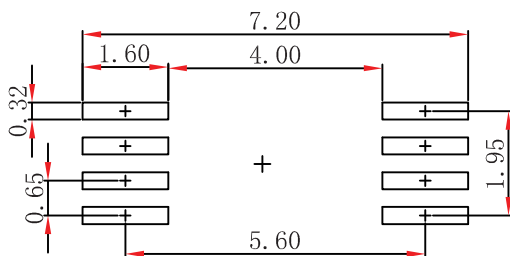
Diode Recovery Test Circuit & Waveforms



TSSOP8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.