

Product Summary

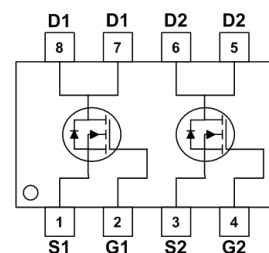
Part #	V_{DS}	$R_{DS(on).typ}$ (@ $V_{GS}=10V$)	$R_{DS(on).typ}$ (@ $V_{GS}=4.5V$)	I_D
EFM4832A	30V	12m Ω	15m Ω	10A

Description

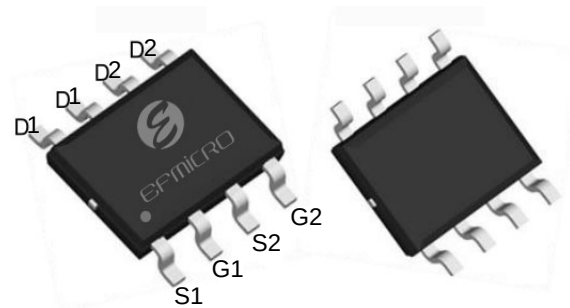
- The EFM4832A is the high cell density trench
- Dual N-ch MOSFETs which provide excellent
- RDSON and gate charge for most of the
- synchronous buck converter applications.
- The EFM4832A meet the RoHS and Green
- Product requirement, 100 % EAS guaranteed
- with full function reliability approved.

Application

- Super Low Gate Charge 100% EAS Guaranteed
- Green Device Available Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



Dual N-Channel MOSFET



SOP-8

Ordering Information:

Part NO.	EFM4832A
Marking	4832 *****
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	10	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	55	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^{\circ}C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	85	$^{\circ}C/W$
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• Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250uA	30	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V V _{GS} =0V	--	--	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V V _{DS} =0V	--	--	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =250uA	1.5	1.9	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V I _D =10A	--	12	14	mΩ
		V _{GS} =4.5V I _D =8A	--	15	18	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V I _D =10A	--	43	--	S
Gate Resistance	R _g	F=1.0MHz	--	1.6	--	Ω
Dynamic Characteristics (Note4)						
Input Capacitance	C _{Iss}	V _{DS} =15V V _{GS} =0V F=1.0MHz	--	760	--	PF
Output Capacitance	C _{Oss}		--	125	--	PF
Reverse Transfer Capacitance	C _{Rss}		--	70	--	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V I _D =10A V _{GS} =10V R _G =3Ω,	--	4.4	--	nS
Turn-on Rise Time	t _r		--	9	--	nS
Turn-Off Delay Time	t _{d(off)}		--	17	--	nS
Turn-Off Fall Time	t _f		--	6	--	nS
Total Gate Charge	Q _g	V _{DS} =15V I _D =10A V _{GS} =10V	--	14	--	nC
Gate-Source Charge	Q _{gs}		--	2.4	--	nC
Gate-Drain Charge	Q _{gd}		--	3	--	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V I _S =10A	--	0.85	1.2	V
Diode Forward Current (Note 2)	I _S		--	--	10	A

Note :

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

• Typical Characteristics

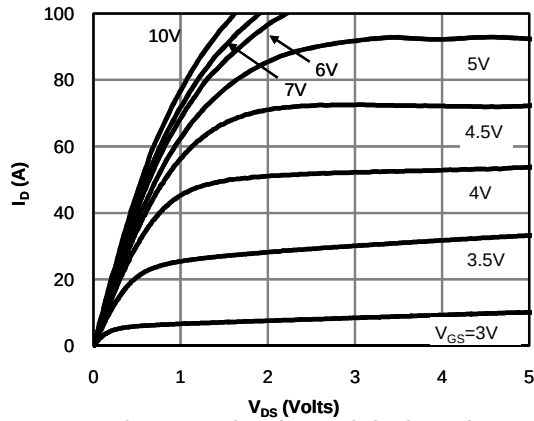


Fig 1: On-Region Characteristics (Note E)

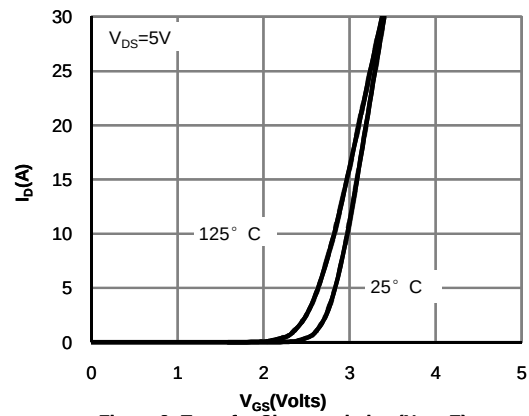


Figure 2: Transfer Characteristics (Note E)

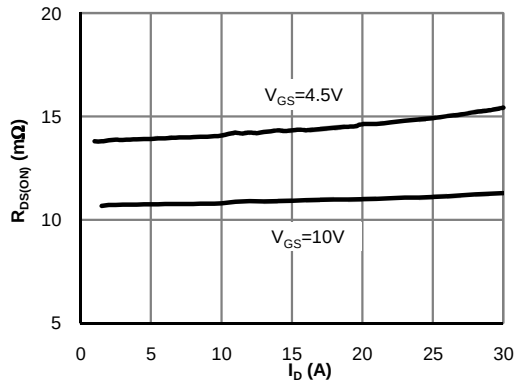


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

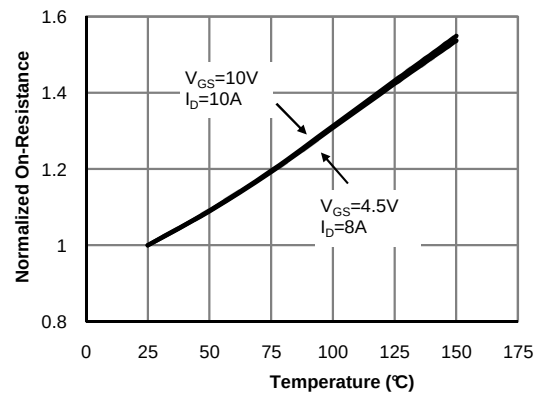


Figure 4: On-Resistance vs. Junction Temperature (Note E)

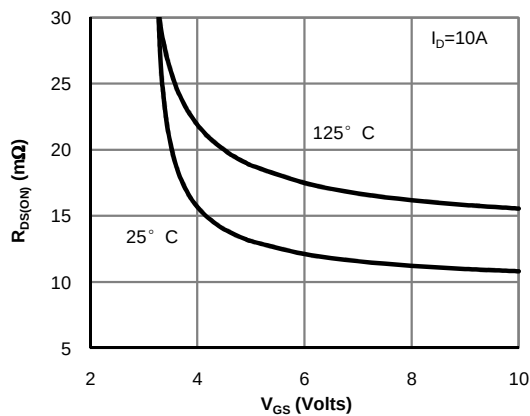


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

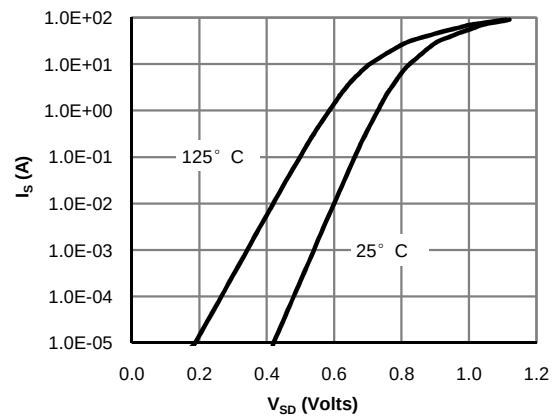


Figure 6: Body-Diode Characteristics (Note E)

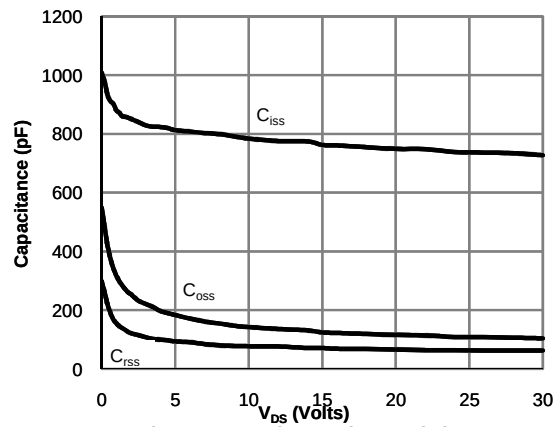
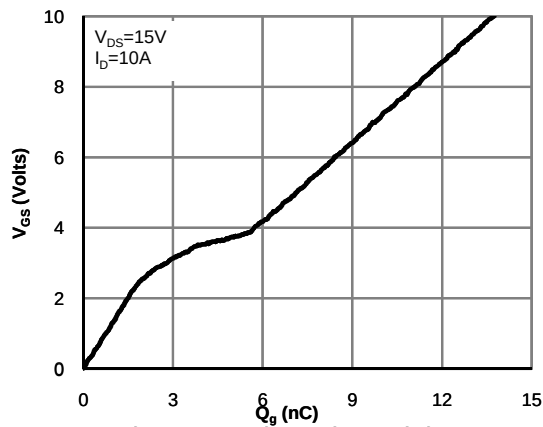


Figure 8: Capacitance Characteristics

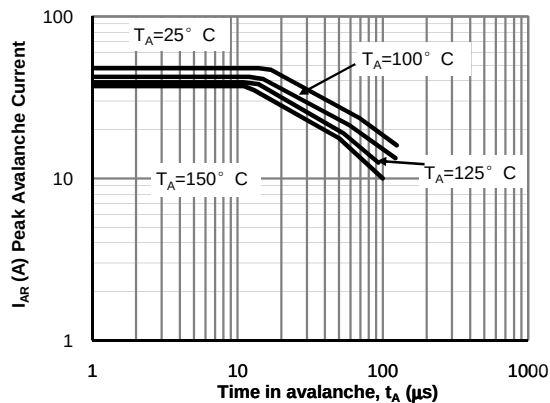


Figure 9: Single Pulse Avalanche capability (Note C)

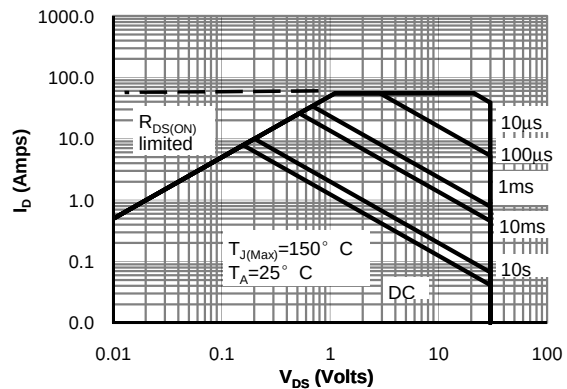


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

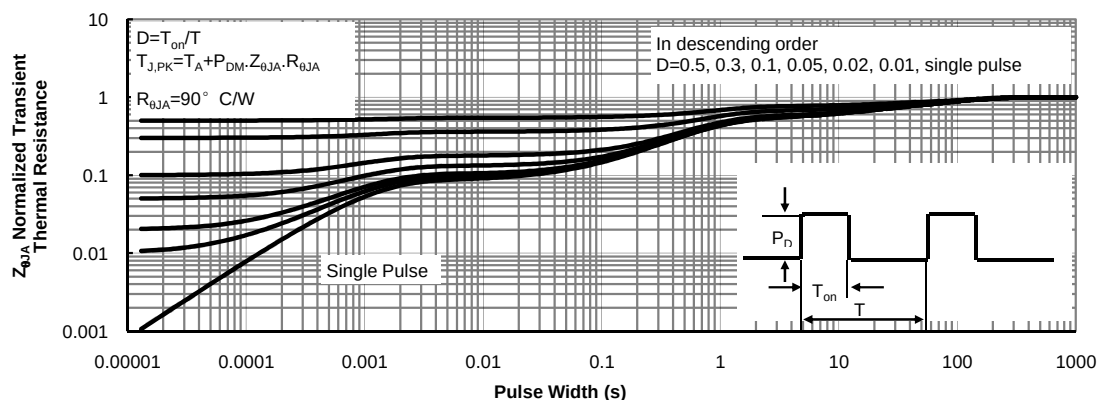
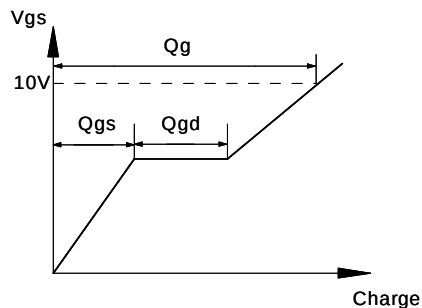
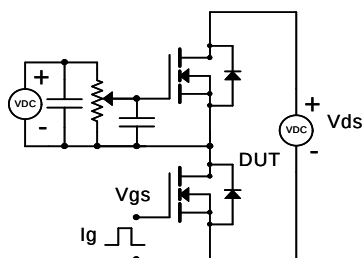


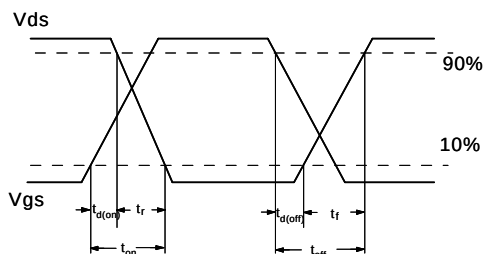
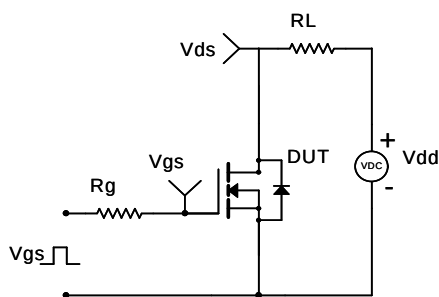
Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

• Test circuit

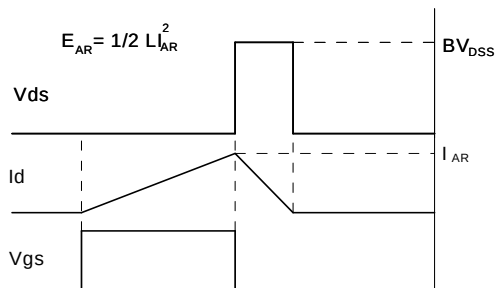
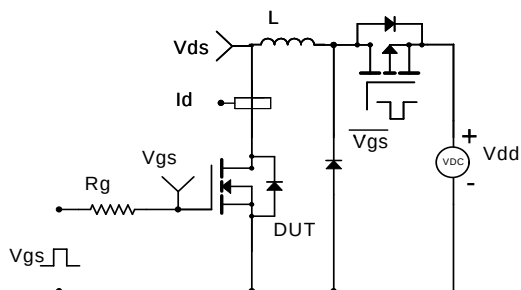
Gate Charge Test Circuit & Waveform



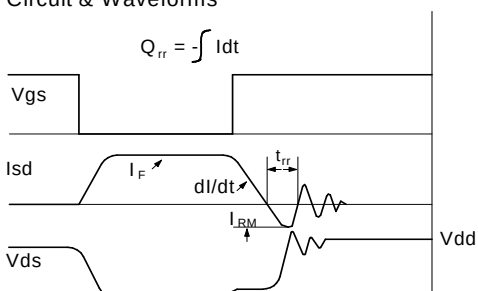
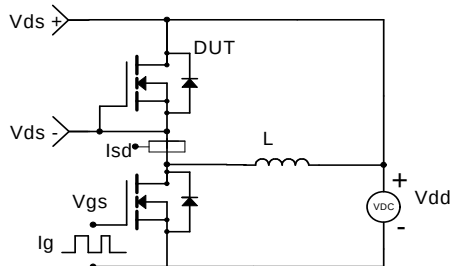
Resistive Switching Test Circuit & Waveforms



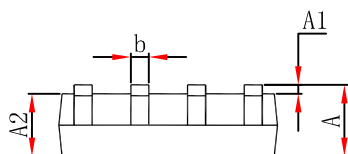
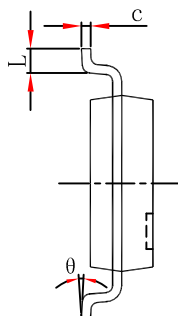
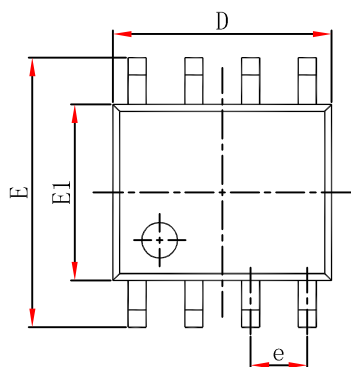
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



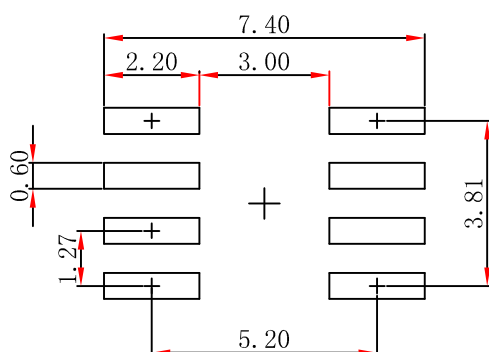
Diode Recovery Test Circuit & Waveforms



SOP8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.