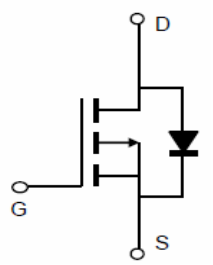
# EFM4485

**P-Channel Advanced MOSFET**

## • Product Summary

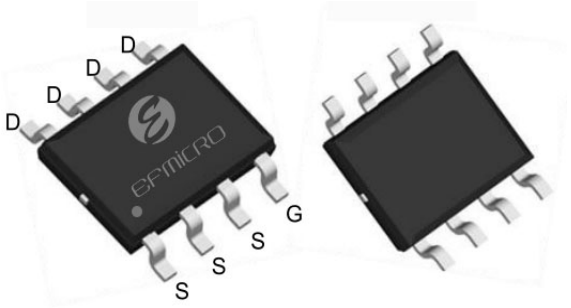
| Part # | $V_{DS}$ | $R_{DS(on).typ}$ (@$V_{GS}$=10V) | $R_{DS(on).typ}$ (@$V_{GS}$=4.5V) | $I_D$ |
|---|---|---|---|---|
| EFM4485 | -40V | 12mΩ | 16mΩ | -12A |




**P-Channel MOSFET**

## • Description

- The EFM4485 is the high cell density trenched
- P-ch MOSFETs which provide excellent
- RDSON and gate cherge for most of the
- synchronous buck converter applications.
- The EFM4485 meet the RoHS and Green
- Prod uct requirement, 100 % EAS guaranteed
- with full function reliability approved.




**SOP-8**

## •Application

- Super Low Gate Charge 100% EAS Guaranteed
- Green Device Available Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

## •Ordering Information:

| | |
|---|---|
| Part NO. | EFM4485 |
| Marking | 4485 ****** |
| Packing Information | REEL TAPE |
| Basic ordering unit (pcs) | 3000 |

## •Absolute Maximum Ratings ($T_C$=25℃)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | -40 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | -12 | A |
| Drain Current-Pulsed (Note 1) | $I_{DM}$ | 52 | A |
| Maximum Power Dissipation | $P_D$ | 3.1 | W |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 150 | ℃ |

## •Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance,Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 41 | ℃/W |

## ● Static Electrical Characteristics @ $T_J$ = 25°C (unless otherwise stated)

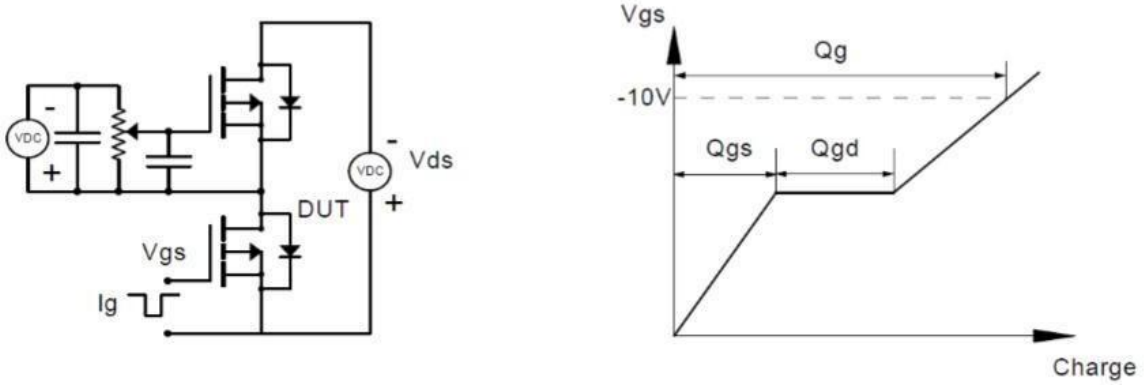
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=250uA | -40 | -- | -- | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-40V $V_{GS}$=0V | -- | -- | -1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V $V_{DS}$=0V | -- | -- | ±100 | nA |
| **On Characteristics** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$ $I_D$=250uA | -1.0 | -1.6 | -2.2 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=-10V $I_D$=-10A | -- | 12 | 15 | mΩ |
| | | $V_{GS}$=-4.5V $I_D$=-8A | -- | 16 | 20 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=-5V $I_D$=-10A | -- | 25 | -- | S |
| Gate Resistance | Rg | F=1.0MHz | -- | 4 | -- | Ω |
| **Dynamic Characteristics** (Note4) | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=-20V $V_{GS}$=0V F=1.0MHz | -- | 2500 | -- | PF |
| Output Capacitance | $C_{oss}$ | | -- | 260 | -- | PF |
| Reverse Transfer Capacitance | $C_{rss}$ | | -- | 180 | -- | PF |
| **Switching Characteristics** (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=-20V $I_D$=-10A $V_{GS}$=-10V $R_G$=3Ω, | -- | 9.4 | -- | nS |
| Turn-on Rise Time | $t_r$ | | -- | 20 | -- | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | -- | 55 | -- | nS |
| Turn-Off Fall Time | $t_f$ | | -- | 30 | -- | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=-20V $I_D$=-10A $V_{GS}$=-10V | -- | 42 | -- | nC |
| Gate-Source Charge | $Q_{gs}$ | | -- | 7 | -- | nC |
| Gate-Drain Charge | $Q_{gd}$ | | -- | 8.6 | -- | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $V_{GS}$=0V $I_S$=-10A | -- | -0.8 | -1.2 | V |
| Diode Forward Current (Note 2) | $I_S$ | | -- | -- | -12 | A |

Note :

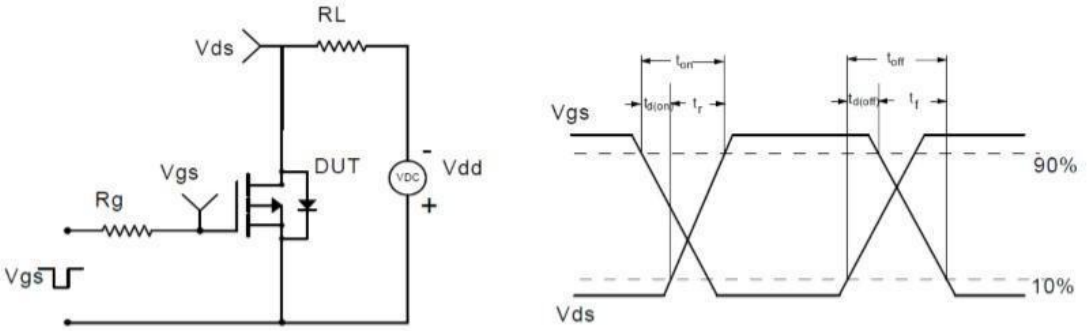
1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is $V_{DD}$= -25V, $V_{GS}$= -10V, L= 0.1mH, $I_{AS}$= -34A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

## • Test Circuit

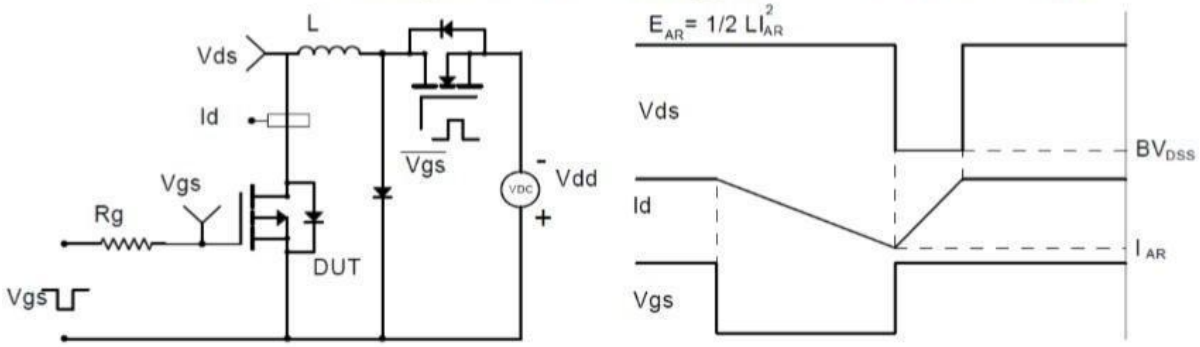
Gate Charge Test Circuit & Waveform



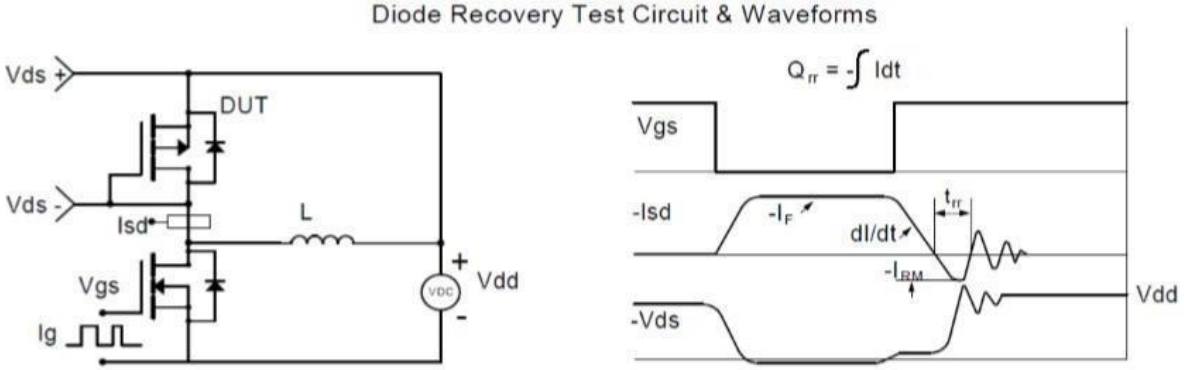

Resistive Switching Test Circuit & Waveforms




Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




Diode Recovery Test Circuit & Waveforms



## • Typical Characteristics

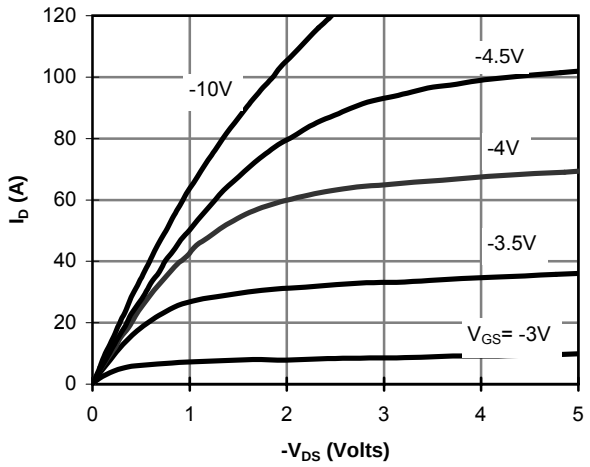



Figure 1: On-Region Characteristics

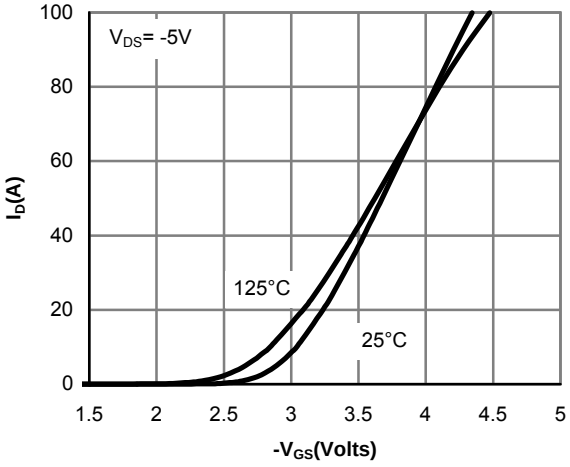



Figure 2: Transfer Characteristics

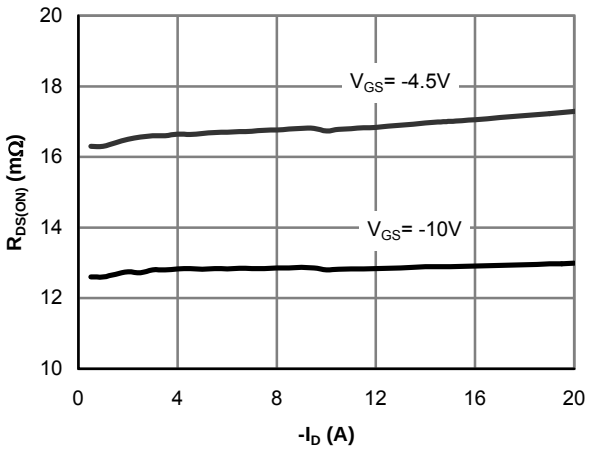



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

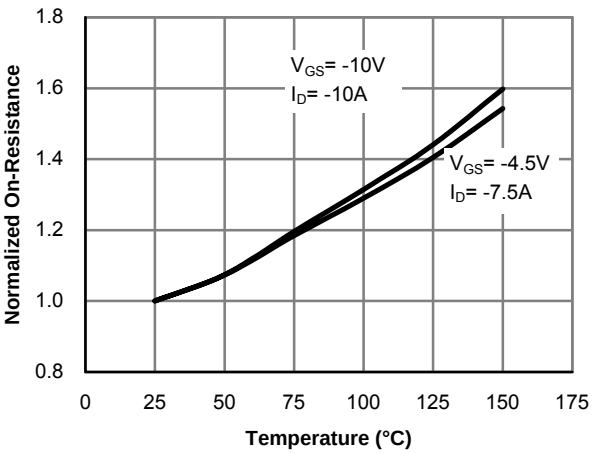



Figure 4: On-Resistance vs. Junction Temperature

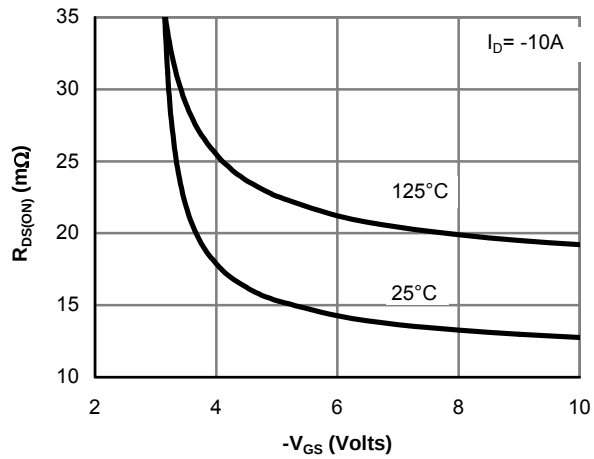



Figure 5: On-Resistance vs. Gate-Source Voltage

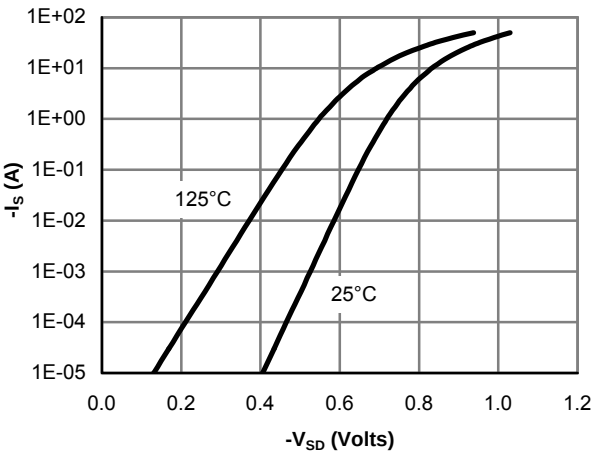



Figure 6: Body-Diode Characteristics

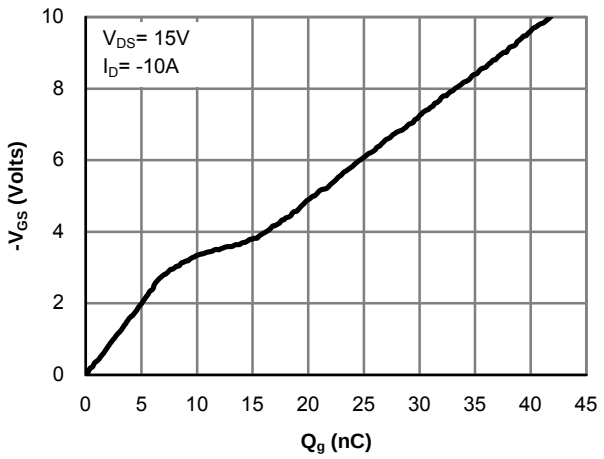



Figure 7: Gate-Charge Characteristics

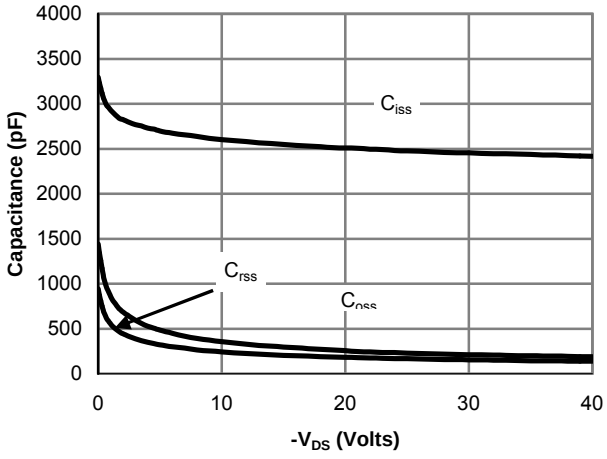



Figure 8: Capacitance Characteristics

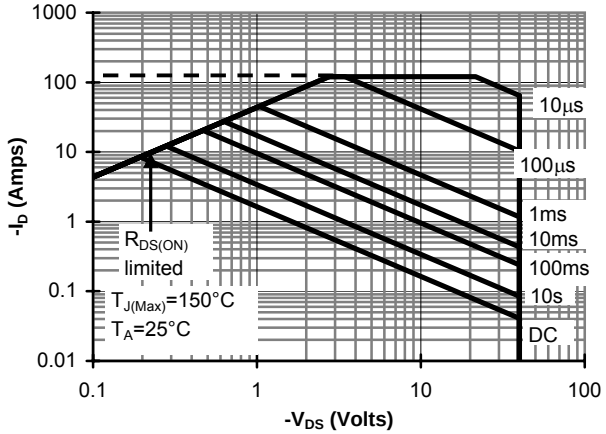



Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

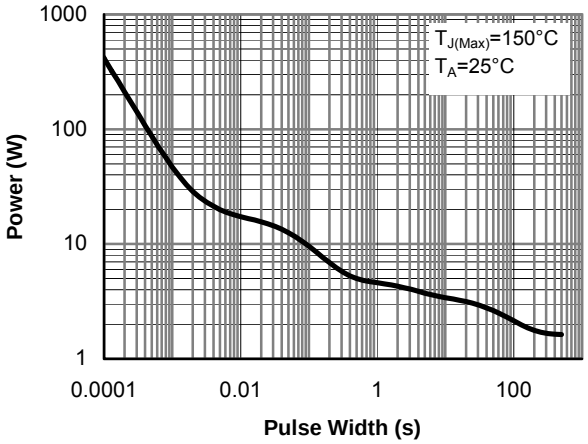



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

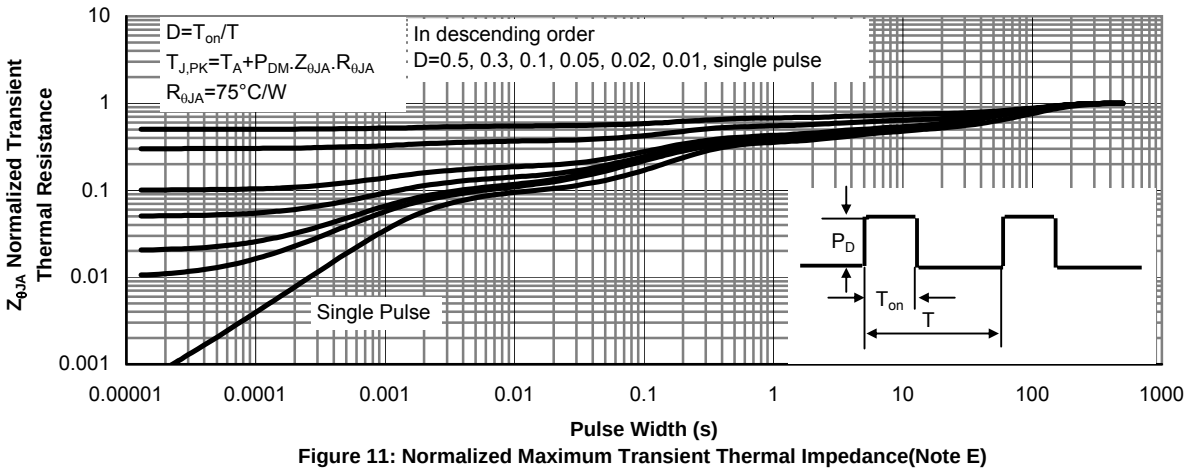
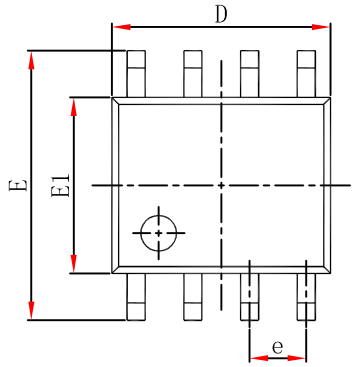
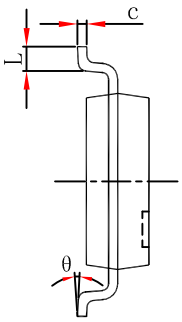
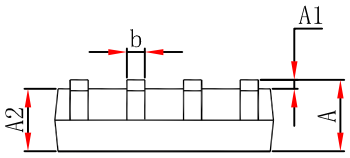



Figure 11: Normalized Maximum Transient Thermal Impedance(Note E)

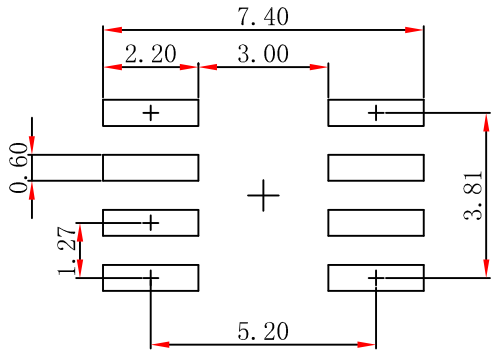
## SOP8 Package Outline Dimensions




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 1.450 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.201 |
| e | 1.270（BSC） | | 0.050（BSC） | |
| E | 5.800 | 6.200 | 0.228 | 0.244 |
| E1 | 3.800 | 4.000 | 0.150 | 0.157 |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |




Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.